REMARKS

The Applicants request reconsideration of the rejection.

Claims 25-30 are pending.

The title of the invention has been amended into a more descriptive form.

The Examiner objected to the drawings as failing to show the step of mounting described in claim 27. Although independent claim 25 and dependent claim 27 have been amended, the Applicants note that the step of mounting the chip on a surface of an inner lead arrangement side of the insulating member is shown in Figures 6 and 7. See also page 22, lines 6 through page 23, line 22 of the specification.

The Applicants have amended the specification to add inequality signs missing from the specification as originally filed. Apparently, the inequality signs did not print due to a software error. No new matter is proposed by these amendments because the verbal description supports the complete inequalities. Other possible informalities have been corrected as well.

Claims 25-27 and 30 stand rejected under 35 U.S.C. §102(b) as being anticipated by Michiyo, JP 05-160304 (Michiyo). Claims 28 and 29 stand rejected under 35 U.S.C.

§103(a) as being unpatentable over Michiyo in view of Fogal et al, U.S. 5,177,032 (Fogal).

Neither Michiyo nor Fogal, however, teaches or fairly suggests the claimed step of mounting a semiconductor chip on the insulating member in each package area, wherein the package area includes a plurality of inner leads and a thin sheet-shaped insulating member joined to an end portion of each of the inner leads and capable of supporting a semiconductor chip. In other words, the prior art does not teach that the semiconductor chip-mounting step is performed with respect to a package area in which the inner leads and insulating member are already joined when the chip is mounted.

By this feature of the invention, movement of the inner leads during the flow of resin at the time of resin sealing is prevented because the inner leads are previously adhered to the insulating member prior to the resin molding. Further, by adhering the ends of the inner leads to the insulating member prior to mounting of the semiconductor chip, the tips of the inner leads can be prevented from movement during the assembling process of the device. By assembling a semiconductor device using the lead frame on which the ends of the inner leads and the thin sheet-shaped insulating member are previously joined, it is also possible to suppress the

expansion and shrinkage of the respective tips of the inner leads at the time of solder reflow caused by thermal expansion coefficient differences between the mold resin and the respective inner leads, which prevents disconnection generated at the joining sections between the wires and inner leads. As a result, the reliability of the semiconductor device can be improved.

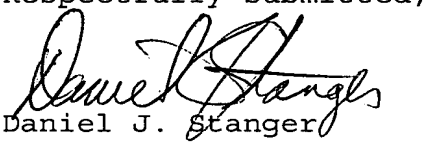
Michiyo does not contain a description of a manufacturing method leading to the device referenced by the Examiner. That is, Michiyo shows a semiconductor device that has excellent heat radiation characteristics in consequence of the structure shown in Figure 1, but Michiyo does not disclose the method for manufacturing the device. Therefore, Michiyo does not provide the person of ordinary skill with any teach or suggestion as to when the inner leads are adhered to the aluminum plate.

Fogal discloses a structure in which a lead frame and a carrier material are attached to each other through one or more layers of thermoplastic, and a die is attached onto the carrier material, but Fogal also does not describe that the leads are attached to the thermoplastic or carrier material prior to the mounting of the die. Therefore, even in

combination with Michiyo, Fogal does not render obvious the claimed invention.

In view of the foregoing amendments and remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



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